

LP87565C-Q1 and TPS65917-Q1 User's Guide to Power DRA7xxP and TDA2Pxx

This user's guide can be used as a guide for integrating both the TPS65917-Q1 and LP87565C-Q1 power-management integrated circuits (PMIC) together into a system powering the DRA7xxP or TDA2Pxx device.

Contents

1	Introduction	2
2	Device Versions	2
3	Platform Connection	3
4	Static Platform Settings	4
4.1	System Voltage Monitoring	4
4.2	Buck and LDO Outputs	5
4.3	Interrupts	6
4.4	GPIO	7
4.5	MISC	9
4.6	SWOFF_HWRST	11
4.7	Shutdown_ColdReset	12
5	Sequence Platform Settings	13
5.1	Power-Up Sequence	13
5.2	Power-Down Sequence	14

List of Figures

1	Processor Connection With O917A154TRGZRQ1 and LP87565CRNFRQ1	3
2	Switch Circuit for TPS65917-Q1 3.3-V VIO_IN	4
3	TPS65917-Q1 State Transitions	5
4	Reset Levels versus Registers	11
5	Power-Up Sequence	13
6	Power-Down Sequence	14

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1 Introduction

This user's guide can be used as a guide for connectivity between both the TPS65917-Q1 and LP87565C-Q1 PMICs and a processor. This guide describes the platform connections as well as the power-up and power-down sequences along with the one-time programmable (OTP) memory configurations. This document does not provide details about the power resources, external components, or the functionality of the devices. For such information, see the [TPS65917-Q1 Power Management Unit \(PMU\) for Processor data sheet](#) and [LP8756-Q1 Four-Phase 16-A Buck Converter with Integrated Switches data sheet](#).

In the event of any inconsistency between the official specification and any user's guide, application report, or other referenced material, the data sheet specification will be the definitive source.

2 Device Versions

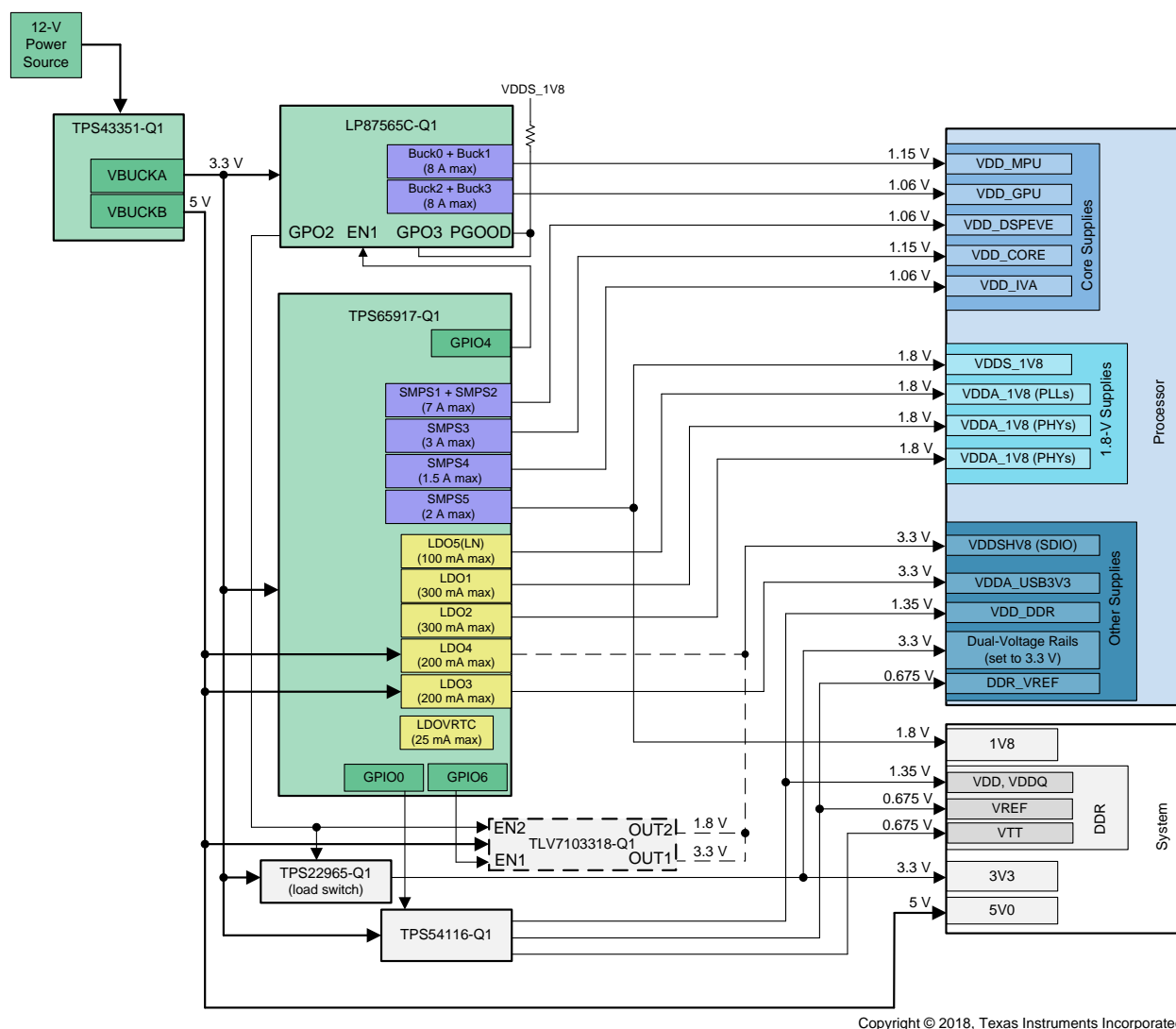
One version of the TPS65917-Q1 device and LP87565C-Q1 device is available and the OTP settings for each version are described in this document. The two devices are used together to power the DRA7xxP and TDA2Pxx processor devices. The OTP version can be read from the device using the SW_REVISION register in the TPS65917-Q1 device and the OTP_REV register in the LP87565C-Q1 device. [Table 1](#) lists the orderable part number and OTP version for each device.

Table 1. Orderable Part Numbers and OTP Versions

ORDERABLE PART NUMBER	OTP Version
O917A154TRGZRQ1	0x54
LP87565CRNFRQ1	0x22

3 Platform Connection

Figure 1 shows the detailed connections between the O917A154TRGZRQ1, LP87565CRNFRQ1, and the processor. This solution is the same power solution used on the DRA7xxP and TDA2Pxx EVMs.



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Figure 1. Processor Connection With O917A154TRGZRQ1 and LP87565CRNFRQ1

The LDO1 and LDO2 regulators of the TPS65917-Q1 device are used to supply the PHY domains. Table 2 lists the processor connections.

Table 2. LDO1 and LDO2 Mapping to PHY Domains

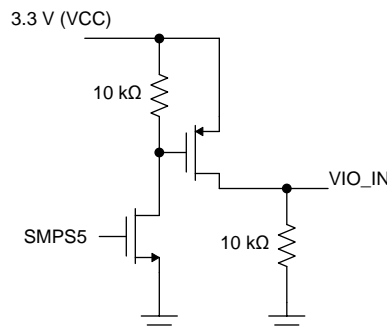
TPS65917-Q1 LDO	PROCESSOR VOLTAGE RAIL
LDO1 (300 mA)	VDDA_CSI
	VDDA_PCIE
	VDDA_PCIE0
	VDDA_PCIE1

Table 2. LDO1 and LDO2 Mapping to PHY Domains (continued)

TPS65917-Q1 LDO	PROCESSOR VOLTAGE RAIL
LDO2 (300 mA)	VDDA_HDMI
	VDDA_SATA
	VDDA_USB1
	VDDA_USB2
	VDDA_USB3

The power solution provides two options to supply VDDSHV8 (SDIO). The first option is for fixed 3.3-V signaling in which case the VDDSHV8 can be powered by the LDO4 regulator. The second option is for dual-voltage 1.8 V and 3.3 V signaling in which case the [TLV7103318-Q1](#) device can be used. In this case, the two outputs of the TLV7103318-Q1 device should be shorted together. The GPIO2 pin of the LP87565C-Q1 device enables the 1.8-V output, and the GPIO_6 pin of the TPS65917-Q1 device enables the 3.3-V output, letting the combined output switch from 1.8 V to 3.3 V as specified for high-speed SD card operations.

The TPS65917-Q1 VIO_IN is the reference voltage for the VIO signals (GPIO_2, GPIO_4, INT, RESET_OUT, and I²C pins). For 1.8-V VIO, SMPS5 can be used to supply VIO_IN. For 3.3-V VIO, a switched version of the 3.3-V supply rail enabled by SMPS5 can be used to supply VIO_IN which allows VIO_IN to be supplied after VCCA, but before GPIO_4 is enabled in the sequence. [Figure 2](#) shows an example of this switch circuit. VIO_IN typically requires 1 μ A during operation.


Figure 2. Switch Circuit for TPS65917-Q1 3.3-V VIO_IN

The [LM5140-Q1](#) device is a similar preregulator to the [TPS43351-Q1](#) device, with a higher switching frequency of 2.2 MHz.

4 Static Platform Settings

Each PMIC device has predefined values stored in the OTP memory which control the default configuration of the device. The tables in this section list the OTP-programmed values for each device.

4.1 System Voltage Monitoring

Table 3. TPS65917-Q1 System Voltage Monitoring OTP Settings

REGISTER	BIT	DESCRIPTION	O917A154TRGZRQ1 VALUE
VSYS_MON	VSYS_HI	System voltage rising-edge threshold	3.1
VSYS_LO	VSYS_LO	System voltage falling-edge threshold	2.75

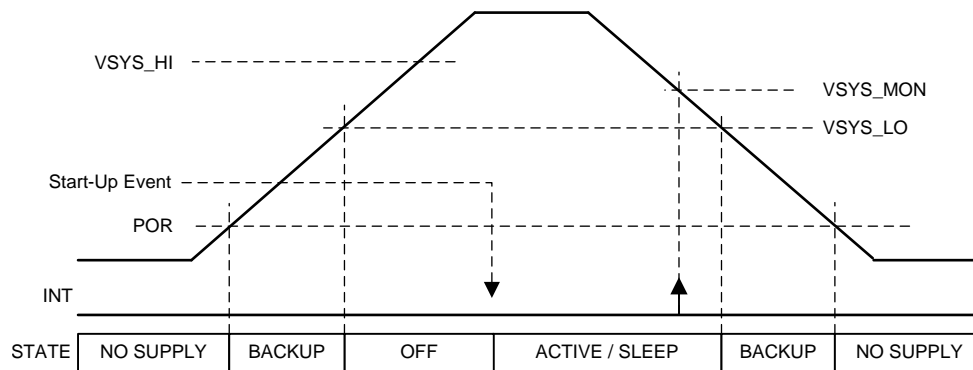


Figure 3. TPS65917-Q1 State Transitions

NOTE: The maximum input voltage of the TPS65917-Q1 VCC_SENSE pin depends on the OTP setting of PMU_CONFIG [HIGH_VCC_SENSE] as listed in the *Recommended Operating Conditions* table of the TPS65917-Q1 data sheet. This configuration is set as HIGH_VCC_SENSE = 0 with the VCC_SENSE pin connected to VCCA.

4.2 Buck and LDO Outputs

This section describes the default voltage and configuration settings for the buck regulators on each device and the LDO regulators on the TPS65917-Q1 device.

Table 4. TPS65917-Q1 SMPS OTP Settings

BIT	DESCRIPTION ⁽¹⁾	0917A154TRGZRQ1 VALUE
SMPS1_VOLTAGE	Default output voltage for the regulator	1.06 V
SMPS2_VOLTAGE	Default output voltage for the regulator	N/A
SMPS3_VOLTAGE	Default output voltage for the regulator	1.15 V
SMPS4_VOLTAGE	Default output voltage for the regulator	1.06 V
SMPS5_VOLTAGE	Default output voltage for the regulator	1.8 V
SMPS1_SMPS12_EN	SMPS12 single-phase or dual-phase configuration. 0b = SMPS1 and SMPS2 single-phase 1b = SMPS12 dual-phase	1

⁽¹⁾ The regulator output voltage cannot be modified while active from one (0.7 to 1.65 V) voltage range to the other (1 to 3.3 V) voltage range or the other way around. The regulator must be turned off to do so.

Table 5. LP87565C-Q1 Buck Regulator OTP Settings

BIT	DESCRIPTION	LP87565CRNFRQ1 VALUE
	Multi-phase configuration of the buck regulators	2 + 2
	Buck regulator switching frequency	2 MHz
BUCK0_VSET	Default output voltage for BUCK0/1	1.15 V
EN_PIN_CTRL0	Enabled by ENx pin, or I ² C register	EN1
EN_BUCK0	Control for BUCK0	Enabled
BUCK0_FPWM_MP	Forces multi-phase for BUCK0/1	0b = Automatic phase adding and shedding
BUCK0_FPWM	Forces BUCK0/1 to operate in PWM mode	1b = Forced PWM mode
SLEW_RATE0	Output voltage slew rate for BUCK0/1	3.8 mV/μs
ILIM0	BUCK0 peak current limit	5 A
ILIM1	BUCK1 peak current limit	5 A
BUCK2_VSET	Default output voltage for BUCK2/3	1.06 V
EN_PIN_CTRL2	Enabled by ENx pin, or I ² C register	EN1
EN_BUCK2	Control for BUCK2	Enabled

Table 5. LP87565C-Q1 Buck Regulator OTP Settings (continued)

BIT	DESCRIPTION	LP87565CRNFRQ1 VALUE
BUCK2_FPWM_MP	Forces multi-phase for BUCK2/3	0b = Automatic phase adding and shedding
BUCK2_FPWM	Forces BUCK2/3 to operate in PWM mode	1b = Forced PWM mode
SLEW_RATE2	Output voltage slew rate for BUCK2/3	3.8 mV/μs
ILIM2	BUCK2 peak current limit	5 A
ILIM3	BUCK3 peak current limit	5 A
EN_SPREAD_SPEC	Enable spread spectrum feature	1b = Enabled

Table 6. TPS65917-Q1 LDO OTP Settings

BIT	DESCRIPTION	O917A154TRGZRQ1 VALUE
LDO1_VOLTAGE	Default output voltage for the regulator	1.8 V
LDO2_VOLTAGE	Default output voltage for the regulator	1.8 V
LDO3_VOLTAGE	Default output voltage for the regulator	3.3 V
LDO4_VOLTAGE	Default output voltage for the regulator	3.3 V
LDO5_VOLTAGE	Default output voltage for the regulator	1.8 V

NOTE: The LDO1 and LDO2 regulators share one input, LDO12_IN, and must be supplied by the same voltage. Refer to the input voltage parameter in the data sheet.

4.3 Interrupts

Each device has multiple interrupt sources, and all interrupts are logically combined on one output line on each device. The TPS65917-Q1 device has an INT pin, and the LP87565C-Q1 device has an nINT pin. Both pins are active low when a pending interrupt occurs. These pins are used as an external interrupt line to inform the host processor of any interrupt event that has occurred within the device. The OTP settings in this section show whether each interrupt is enabled or disabled by default.

Table 7. TPS65917-Q1 Interrupt OTP Settings

REGISTER	BIT	DESCRIPTION	O917A154TRGZRQ1 VALUE
INT1_MASK	VSYS_MON	Enable and disable interrupt from the VSYS_MON comparator	1b = Interrupt generation disabled
	PWRDOWN	Enable and disable interrupt from the PWRDOWN pin	1b = Interrupt generation disabled
	PWRON	Enable and disable interrupt from PWRON pin. A PWRON event is always an ON request.	1b = Interrupt generation disabled
	LONG_PRESS_KEY	Enable and disable interrupt from long key press on the PWRON pin	1b = Interrupt generation disabled
	HOTDIE	Enable and disable interrupt from device hot-die detection. The interrupt can be used as a pre-warning for processor to limit the PMIC load, before increasing die temperature forces shutdown.	0b = Interrupt generated
INT2_MASK	SHORT	Triggered from internal event of SMPS or LDO outputs failing. If an interrupt is enabled, it is an ON request.	0b = Interrupt generated
	WDT	Enable and disable interrupt from watchdog expiration	1b = Interrupt generation disabled
	FSD	Enable and disable First Supply Detection (FSD) interrupt	1b = Interrupt generation disabled
	RESET_IN	Enable and disable interrupt from the RESET_IN pin	1b = Interrupt generation disabled
INT3_MASK	VBUS	Interrupt to detect rising or falling VBUS line	1b = Interrupt generation disabled
	GPADC_EOC_SW	GPADC result ready from software-initiated conversion	1b = Interrupt generation disabled
	GPADC_AUTO_1	GPADC automatic conversion result 1 above or below the reference threshold	1b = Interrupt generation disabled
	GPADC_AUTO_0	GPADC automatic conversion result 0 above or below the reference threshold	1b = Interrupt generation disabled
INT4_MASK	GPIO_6	Enable and disable interrupt from the GPIO6 pin rising or falling edge	1b = Interrupt generation disabled
	GPIO_5	Enable and disable interrupt from the GPIO5 pin rising or falling edge	1b = Interrupt generation disabled
	GPIO_4	Enable and disable interrupt from the GPIO4 pin rising or falling edge	1b = Interrupt generation disabled
	GPIO_3	Enable and disable interrupt from the GPIO3 pin rising or falling edge	1b = Interrupt generation disabled
	GPIO_2	Enable and disable interrupt from the GPIO2 pin rising or falling edge	1b = Interrupt generation disabled
	GPIO_1	Enable and disable interrupt from the GPIO1 pin rising or falling edge	1b = Interrupt generation disabled
	GPIO_0	Enable and disable interrupt from the GPIO0 pin rising or falling edge	1b = Interrupt generation disabled

Table 8. LP87565C-Q1 Interrupt OTP Settings

REGISTER	BIT	DESCRIPTION	LP87565CRNFRQ1 VALUE
TOP_MASK	SYNC_CLK_MASK	Enable and disable interrupt for the external clock detection	1b = Interrupt generation disabled
	TDIE_WARN_MASK	Enable and disable interrupt for the thermal warning	0b = Interrupt generated
	I_LOAD_READY_MASK	Enable and disable interrupt for load current measurement ready	1b = Interrupt generation disabled
TOP_MASK2	RESET_REG_MASK	Enable and disable interrupt for register reset	1b = Interrupt generation disabled
BUCK_0_1_MASK	BUCK0_PG_MASK	Enable and disable interrupt for BUCK0 power good	1b = Interrupt generation disabled
	BUCK0_ILIM_MASK	Enable and disable interrupt for BUCK0 current limit detection	0b = Interrupt generated
	BUCK1_PG_MASK	Enable and disable interrupt for BUCK1 power good	1b = Interrupt generation disabled
	BUCK1_ILIM_MASK	Enable and disable interrupt for BUCK1 current limit detection	0b = Interrupt generated
BUCK_2_3_MASK	BUCK2_PG_MASK	Enable and disable interrupt for BUCK2 power good	1b = Interrupt generation disabled
	BUCK2_ILIM_MASK	Enable and disable interrupt for BUCK2 current limit detection	0b = Interrupt generated
	BUCK3_PG_MASK	Enable and disable interrupt for BUCK3 power good	1b = Interrupt generation disabled
	BUCK3_ILIM_MASK	Enable and disable interrupt for BUCK3 current limit detection	0b = Interrupt generated

4.4 GPIO

The TPS65917-Q1 device integrates seven configurable general-purpose I/Os (GPIOs) that are multiplexed with alternative features. This section describes the default configuration of each GPIO, as well as the configuration of internal pullup or pulldown resistors on the GPIOs.

Table 9. TPS65917-Q1 GPIO OTP Settings

REGISTER	BIT	DESCRIPTION	O917A154TRGZRQ1 VALUE
PRIMARY_SECONDARY_PAD2	GPIO_6	Select pin function	REGEN3
	GPIO_5	Select pin function	POWERHOLD
	GPIO_4	Select pin function	REGEN2
PRIMARY_SECONDARY_PAD1	GPIO_3	Select pin function	SYNCD CDC
	GPIO_2	Select pin function	GPIO_2
	GPIO_1	Select pin function	NRESWARM
	GPIO_0	Select pin function	REGEN1

NOTE: The GPIO_0 and GPIO_6 pins are open-drain pins and therefore must be pulled up externally. TI does not recommend pulling these pins up to any always-on signal such as VCCA or LDOVRTC_OUT. The GPIO_0 and GPIO_6 pins are configured as inputs before the OTP memory is loaded at power up, and pulling the pin up to an always-on rail can cause a glitch on these pins. Therefore, TI recommends pulling this signal up to a sequenced output, such as SMPS5 (1.8 V) or LDO4 (3.3 V).

The LP87565C-Q1 device integrates three GPIOs which can be configured as a GPIO function or an enable function as described in [Table 10](#).

Table 10. LP87565C-Q1 GPIO OTP Settings

REGISTER	BIT	DESCRIPTION	LP87565CRNFRQ1 VALUE
PIN_FUNCTION	GPIO1_SEL	Select pin function	EN1
	GPIO2_SEL	Select pin function	GPIO2
	GPIO3_SEL	Select pin function	GPIO3
	EN_PIN_SELECT_GPIO2	Pin control for GPIO2	0b = EN1
	EN_PIN_CTRL_GPIO2	Enabled by ENx pin, or I ² C register	1b = EN1
	EN_PIN_SELECT_GPIO3	Pin control for GPIO3	0b = EN1
	EN_PIN_CTRL_GPIO3	Enabled by ENx pin, or I ² C register	1b = EN1
GPIO_OUT	GPIO1_OUT	Default state of GPIO output	0b = Low
	GPIO2_OUT	Default state of GPIO output	0b = Low
	GPIO3_OUT	Default state of GPIO output	0b = Low
GPIO_CONFIG	GPIO1_OD	Select signal type when configured as output	1b = Open-drain
	GPIO1_DIR	Select signal direction when configured as GPIO	1b = Output
	GPIO2_OD	Select signal type when configured as output	0b = Push-pull
	GPIO2_DIR	Select signal direction when configured as GPIO	1b = Output
	GPIO3_OD	Select signal type when configured as output	0b = Open-drain
	GPIO3_DIR	Select signal direction when configured as GPIO	1b = Output

Table 11 describes the pullup, pulldown, and open-drain settings for the corresponding TPS65917-Q1 GPIOs. These settings only apply in GPIO mode (for example, GPIO_0), and do not apply to any of the secondary functions (for example, REGEN1).

Table 11. TPS65917-Q1 GPIO Pullup, Pulldown, and Open Drain Settings

REGISTER	BIT	DESCRIPTION	O917A154TRGZRQ1 VALUE
PU_PD_GPIO_CTRL2	GPIO_6_PD	Configure pulldown for GPIO_6	0b = Pulldown disabled
	GPIO_5_PD	Configure pulldown for GPIO_5	0b = Pulldown disabled
	GPIO_4_PU	Configure pullup for GPIO_4	0b = Pullup disabled
	GPIO_4_PD	Configure pulldown for GPIO_4	0b = Pulldown disabled
PU_PD_GPIO_CTRL1	GPIO_3_PD	Configure pulldown for GPIO_3	1b = Pulldown enabled
	GPIO_2_PU	Configure pullup for GPIO_2	1b = Pullup enabled
	GPIO_2_PD	Configure pulldown for GPIO_2	0b = Pulldown disabled
	GPIO_1_PD	Configure pulldown for GPIO_1	0b = Pulldown disabled
	GPIO_0_PD	Configure pulldown for GPIO_0	0b = Pulldown disabled
OD_OUTPUT_GPIO	GPIO_4_OD	Configure GPIO_4 to be open-drain or push-pull	0b = Push-pull
	GPIO_2_OD	Configure GPIO_2 to be open-drain or push-pull	0b = Push-pull

Table 12 describes the polarity settings for each TPS65917-Q1 GPIO. These settings apply to both GPIO mode and secondary functions.

Table 12. GPIO Polarity Settings

REGISTER	BIT	DESCRIPTION	O917A154TRGZRQ1 VALUE
POLARITY_CTRL	GPIO_6_POLARITY	Enable or disable polarity inversion for GPIO_6	0b = Inversion disabled
	GPIO_5_POLARITY	Enable or disable polarity inversion for GPIO_5	0b = Inversion disabled
	GPIO_4_POLARITY	Enable or disable polarity inversion for GPIO_4	0b = Inversion disabled
	GPIO_3_POLARITY	Enable or disable polarity inversion for GPIO_3	0b = Inversion disabled
	GPIO_2_POLARITY	Enable or disable polarity inversion for GPIO_2	0b = Inversion disabled
	GPIO_1_POLARITY	Enable or disable polarity inversion for GPIO_1	0b = Inversion disabled
	GPIO_0_POLARITY	Enable or disable polarity inversion for GPIO_0	0b = Inversion disabled

4.5 MISC

This section describes miscellaneous device configuration settings including pulldowns, polarity of signals, communication settings, and other functionality.

Table 13. TPS65917-Q1 Miscellaneous OTP Settings

REGISTER	BIT	DESCRIPTION	O917A154TRGZRQ1 VALUE
PU_PD_INPUT_CTRL1	RESET_IN_PD	Enable and disable internal pulldown for the RESET_IN pin	1b = Pulldown enabled
	PWRDOWN_PD	Enable and disable internal pulldown for the PWRDOWN pin	1b = Pulldown enabled
I2C_SPI	I2C_SPI	Selection of control interface, I ² C, or SPI	0b = I ² C
	ID_I2C2	I2C_2 address for page access versus initial address (0H12)	0b = Address is 0x12
	ID_I2C1	I2C_1 address for I ² C register access	I2C_1[0] = 1b = 0x58 I2C_1[1] = 1b = 0x59 I2C_1[2] = 1b = 0x5A I2C_1[3] = 1b = 0x5B
PMU_CONFIG	HIGH_VCC_SENSE	Enable internal buffers on VCC_SENSE to allow voltage sensing above 5.25 V	0b = High VCC sense not enabled
	AUTODEVON	Automatically set DEV_ON bit after startup sequence completes	0b = AUTODEVON disabled
	SWOFF_DLY	Delay before switch-off to let host processor save context. Device stays in the ACTIVE state until delay expiration then switches off.	00b = No delay
PMU_CTRL2	INT_LINE_DIS	Configure INT output to be standard buffer or high-impedance buffer with pullup to VIO	0b = Standard buffer: open-drain or push-pull
	WDT_HOLD_IN_SLEEP	Configure watchdog timer operation during device sleep state	0b = Watchdog timer continues to run in sleep state
	PWRDOWN_FASTOFF	Configure shut-down sequence from PWRDOWN pin event	0b = PWRDOWN pin event triggers sequenced shut down
	TSHUT_FASTOFF	Configure shut-down sequence from thermal shutdown event	0b = Thermal shutdown triggers sequenced shut down
OD_OUTPUT_CTRL2	RESET_OUT_OD	Configure RESET_OUT to be push-pull or open-drain	0b = RESET_OUT is push-pull
	REGEN2_OD	Configure REGEN2 to be push-pull or open-drain	0b = REGEN2 is push-pull
PMU_SECONDARY_INT	FSD_MASK	Secondary level of mask for FSD interrupt line	1b = FSD_INT_SRC is masked
POLARITY_CTRL	INT_POLARITY	Configure polarity of INT line	0b = INT line is low when interrupt is pending
PRIMARY_SECONDARY_PAD2	SYNCLKOUT	Configure SYNCLKOUT to output SYNCDCDCCLK or CLK32KGO	0b = SYNCDCDCCLK

Table 14. LP87565C-Q1 Miscellaneous OTP Settings

REGISTER	BIT	DESCRIPTION	LP87565CRNFRQ1 VALUE
PGOOD_CTRL1	PG0_SEL	PGOOD monitoring of BUCK0	Voltage and current
	PG1_SEL	PGOOD monitoring of BUCK1	Voltage and current
	PG2_SEL	PGOOD monitoring of BUCK2	Voltage and current
	PG3_SEL	PGOOD monitoring of BUCK3	Voltage and current
PGOOD_CTRL2	EN_PG0_INT	Include BUCK0 PGOOD in the nINT signal	0b = BUCK0 not included in nINT
	PGOOD_SET_DELAY	Debounce time of output voltage monitoring for PGOOD signal	0b = 4 μ s to 8 μ s
	EN_PGFLT_STAT	Operation mode of PGOOD signal	0b = Live status of monitored outputs
	PGOOD_WINDOW	Monitoring method of PGOOD signal	1b = Overvoltage and undervoltage
	PGOOD_OD	PGOOD output type	1b = Open-drain
	PGOOD_POL	PGOOD Polarity	0b = PGOOD high when outputs are valid
PLL_CTRL	PLL_MODE	Selection of PLL operation	00b = PLL Disabled
	EXT_CLK_FREQ	Frequency of external clock (CLKIN)	13h = 20 MHz
CONFIG	CLKIN_PD	Selects the pull down resistor on CLKIN pin	1b = Enabled
	EN4_PD	Selects the pull down resistor on EN4 pin	0b = Disabled
	EN3_PD	Selects the pull down resistor on EN3 pin	0b = Disabled
	EN2_PD	Selects the pull down resistor on EN2 pin	0b = Disabled
	EN1_PD	Selects the pull down resistor on EN1 pin	1b = Enabled
	TDIE_WARN_LEVEL	Thermal warning threshold level	1b = 140°C
	HALF_DELAY, DOUBLE_DELAY	Selects the step size for startup and shutdown delays	0b = 10 ms, 0.64-ms steps
		Input overvoltage protection	Enabled
		I ² C slave address	0x60

4.6 SWOFF_HWRST

This section describes whether each reset type of the TPS65917-Q1 device is configured to generate a HWRST or SWORST. The resets are defined as follows:

Hardware reset (HWRST) — A hardware reset occurs when any OFF request is configured to generate a hardware reset. This reset triggers a transition to the OFF state from either the ACTIVE or SLEEP state (execute either the ACT2OFF or SLP2OFF sequence).

Switch-off reset (SWORST) — A switch-off reset occurs when any OFF request is configured to not generate a hardware reset. This reset acts as the HWRST, except only the SWO registers are reset. The device goes to the OFF state, from either ACTIVE or SLEEP, and therefore executes the ACT2OFF or SLP2OFF sequence.

The power resource control registers for SMPS and LDO voltage levels and operating mode control are in SWORST domain. Additionally some registers control the 32-kHz, REGENx and SYSENx, watchdog, and VSYS_MON comparator. This list is indicative only.

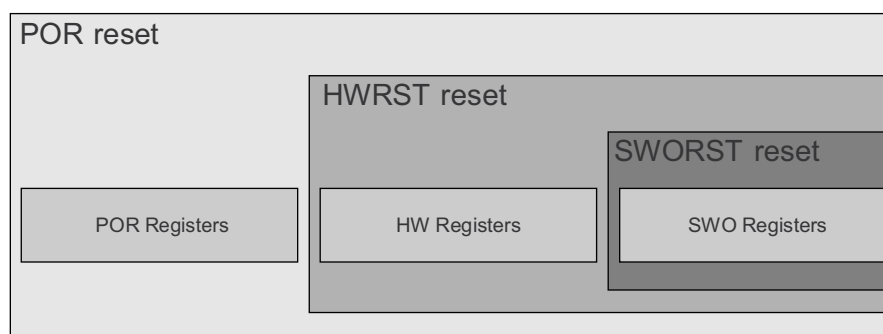


Figure 4. Reset Levels versus Registers

Table 15. SWOFF_HWRST OTP Settings

REGISTER	BIT	DESCRIPTION	O917A154TRGZRQ1 VALUE
SWOFF_HWRST	PWRON_LPK	Define if PWRON long key press is causing HWRST or SWORST	1b = HWRST
	PWRDOWN	Define if PWRDOWN pin is causing HWRST or SWORST	0b = SWORST
	WTD	Define if watchdog expiration is causing HWRST or SWORST	1b = HWRST
	TSHUT	Define if thermal shutdown is causing HWRST or SWORST	1b = HWRST
	RESET_IN	Define if RESET_IN pin is causing HWRST or SWORST	1b = HWRST
	SW_RST	Define if register bit is causing HWRST or SWORST	1b = HWRST
	VSYS_LO	Define if VSYS_LO is causing HWRST or SWORST	1b = HWRST
	GPADC_SHUTDOWN	Define if GPADC event is causing HWRST or SWORST	0b = SWORST

4.7 Shutdown_ColdReset

These OTP settings show whether each OFF request of the TPS65917-Q1 device is configured to generate a shutdown request (SD) or cold reset request (CR). When configured to generate an SD, the embedded power controller (EPC) executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and stays in the OFF state. When configured to generate a CR, the EPC executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and restarts, going to the ACTIVE state (OFF2ACT power sequence) if none of the ON request gating conditions are present.

Table 16. Shutdown_ColdReset OTP Settings

REGISTER	BIT	DESCRIPTION	0917A154TRGZRQ1 VALUE
SWOFF_COLDRST	PWRON_LPK	Define if PWRON long key press causes shutdown or cold reset	0b = Shutdown
	PWRDOWN	Define if PWRDOWN pin causes shutdown or cold reset	0b = Shutdown
	WTD	Define if watchdog timer expiration causes shutdown or cold reset	1b = Cold reset
	TSHUT	Define if thermal shutdown causes shutdown or cold reset	0b = Shutdown
	RESET_IN	Define if RESET_IN pin causes shutdown or cold reset	0b = Shutdown
	SW_RST	Define if SW_RST register bit causes shutdown or cold reset	1b = Cold reset
	VSYS_LO	Define if VSYS_LO causes shutdown or cold reset	0b = Shutdown
	GPADC_SHUTDOWN	Define if GPADC shutdown causes shutdown or cold reset	0b = Shutdown

5 Sequence Platform Settings

A power sequence is an automatic preprogrammed sequence supported by the TPS65917-Q1 and LP87565C-Q1 devices to enable or disable the device outputs.

5.1 Power-Up Sequence

When an ON request occurs while the TPS65917-Q1 device is in the OFF state, the device is switched on and each resource is enabled based on the programmed power up sequence.

Figure 5 shows the power-up sequence of the power solution. The timings in the diagram have $\pm 10\%$ variation.

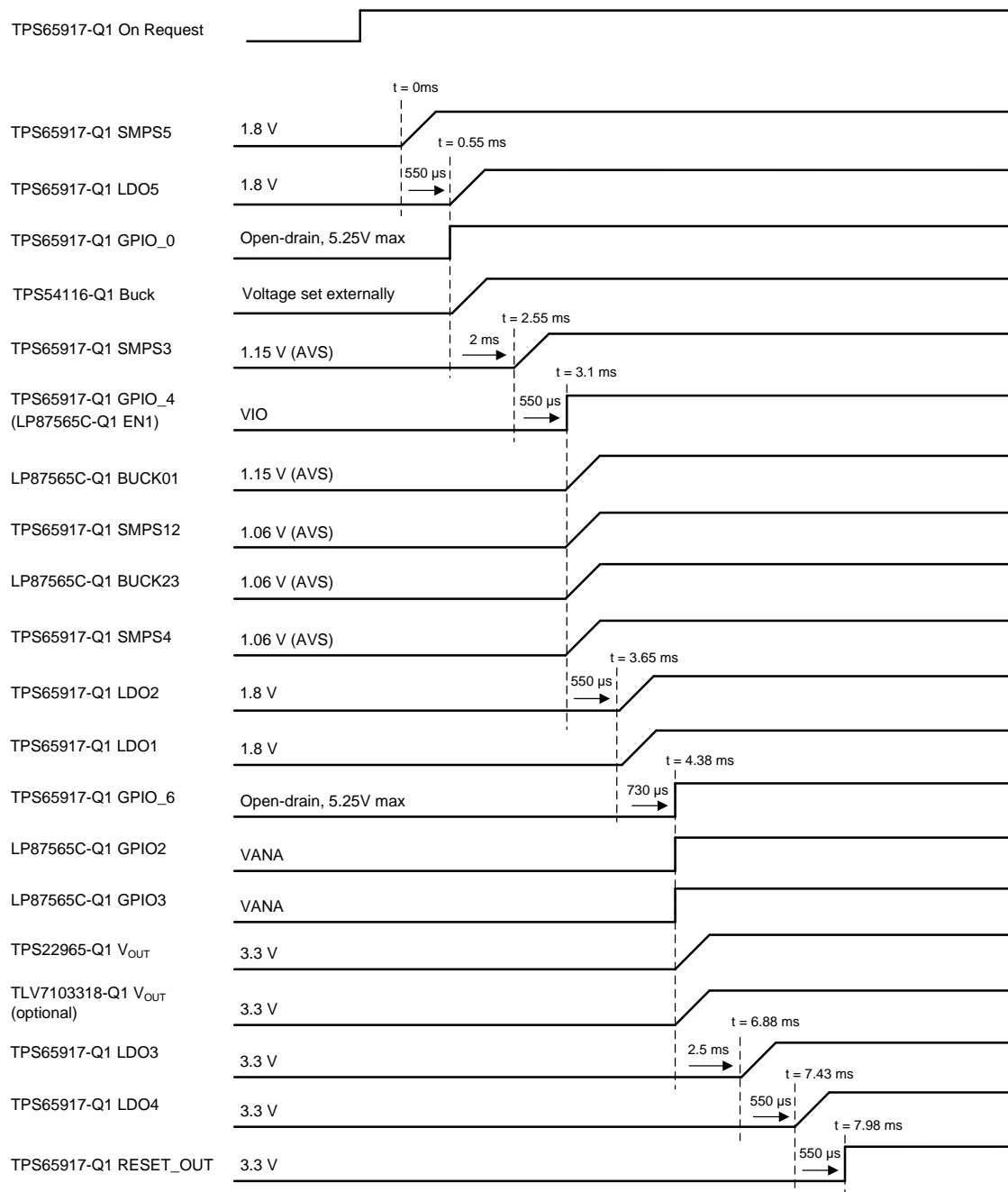


Figure 5. Power-Up Sequence

5.2 Power-Down Sequence

When an OFF request occurs while the TPS65917-Q1 device is in the ACTIVE state, each resource is disabled based on the programmed power down sequence.

Figure 6 shows the power-down sequence of the power solution. The timings in the diagram have $\pm 10\%$ variation.

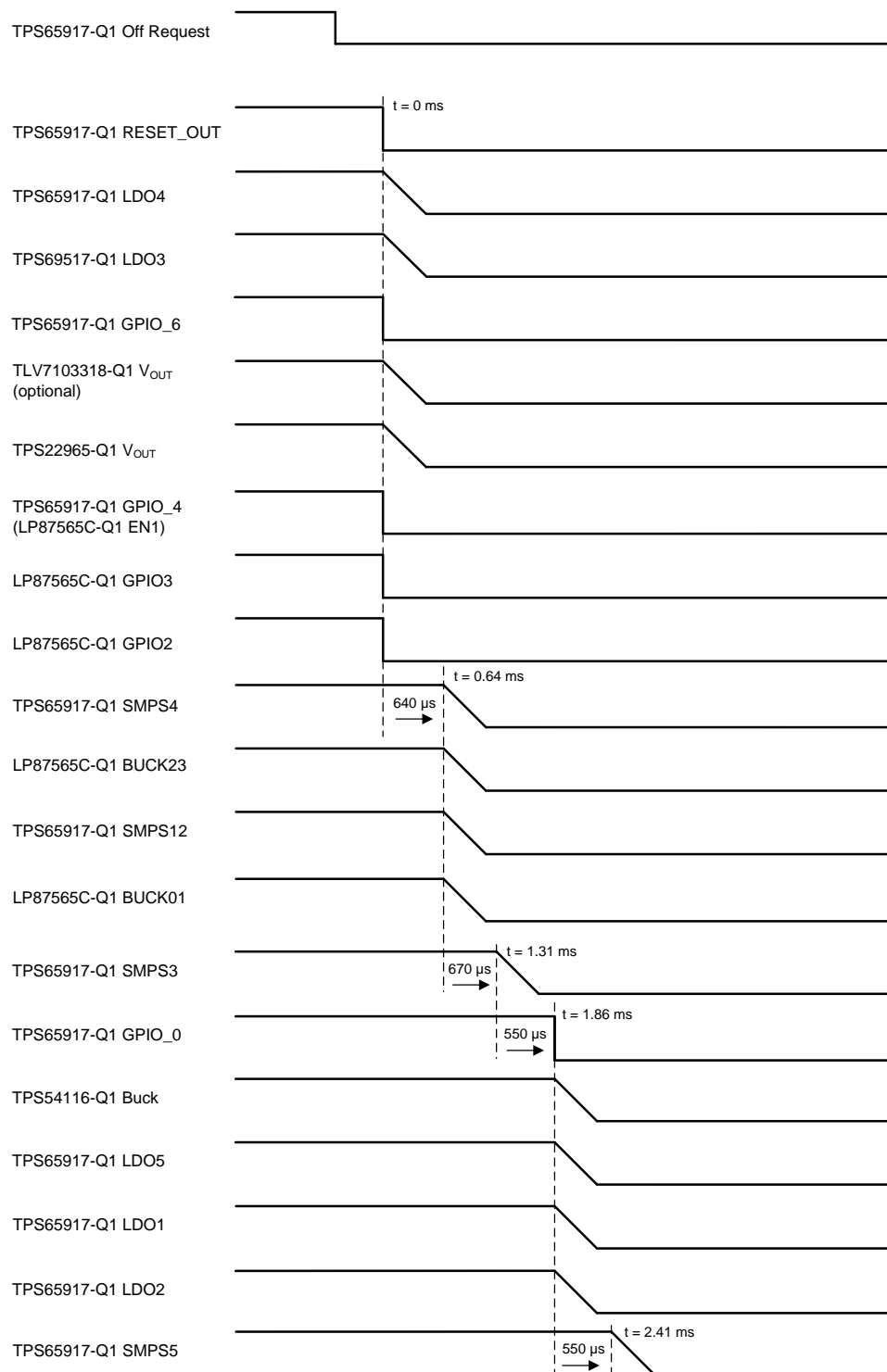


Figure 6. Power-Down Sequence

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2018) to A Revision	Page
<ul style="list-style-type: none"> Corrected the <i>Power-Up Sequence</i> figure (removed delay between TPS65917-Q1 GPIO_4 and LP87565C-Q1 BUCK01) 13 Corrected the <i>Power-Down Sequence</i> figure (delay before TPS65917-Q1 SMPS3 changed to 670 μs and delay before TPS65917-Q1 LDO1 removed) 14 	

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